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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/890,816	08/01/2001	Neil Lightowler	740789-051830	7941

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EXAMINER	
HOLMES, MICHAEL B	

ART UNIT	PAPER NUMBER
2121	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/890,816	LIGHTOWLER, NEIL	
	Examiner	Art Unit	
	Michael B. Holmes	2121	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *(3)* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 August 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14 and 16-21* is/are rejected.

7)☒ Claim(s) *15, 22 and 23* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 August 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/890,816.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *01212003*.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *Detailed Office Action*.

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Examiner's Detailed Office Action

1. This Office Action is responsive to application 09/890,816, filed August 01, 2001.

2. Claims 1-23 have been examined.

Specification Objection(s)

3. The claims contained figure numbers which will need to be removed. The rationale is that over time figures and figure number can change, and thus, should be excluded from the claim language.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1, 2, 7, 10, 12-14 & 17 are rejected under 35 U.S.C. 102(b) as being anticipated by *Masuda et al.* (USPN 5,165,010).

Regarding claim 1. *Masuda et al.* teaches a neural processing element for use in a neural network [*see* C 2, L 35-48], the processing element comprising: arithmetic logic means [*see* Fig. 22, C 26, L 57 to C 27, L 28]; an arithmetic shifter mechanism [*see* Fig. 22, item 807]; data multiplexing means [*see* Fig. 23, C 28, L 45-54]; memory means [*see* Fig. 22, item 101]; data input means including at least one input port [*see* Fig. 2, item 300]; data output means including at least one output port [*see* Fig. 2, item 300]; and control logic means [*see* Fig. 22, C 26, L 57 to C 27, L 28].

Regarding claim 2. *Masuda et al.* teaches a each neural processing element is a single neuron in the neural network [*see* Fig. 3, item 100, C 6, 34-44].

Regarding claim 7. *Masuda et al.* teaches control logic means [*see* Fig. 22, C 26, L 57 to C 27, L 28]; data input means including at least one input port [*see* Fig. 2, item 300]; data output means including at least one output port [*see* Fig. 2, item 300]; data multiplexing means [*see* Fig. 23, C 28, L 45-54]; memory means [*see* Fig. 22, item 101]; an address map [*see* C 18, L 56 to C 19, L 52]; and at least one handshake mechanism [*see* C 4, L 17-34 & Fig. 13, C 17, L 40 to C 19, L 52].

Regarding claim 10. *Masuda et al.* teaches a neural network module comprising an array of neural processing [*see* C 4, L 3-11 & Fig. 9] elements as claimed in claim 1; and at least one neural network controller [*see* Fig. 7, item 200, C 11, L 39 to C 12, L 16] as claimed in claim 7.

Regarding claim 12. *Masuda et al.* teaches a module as claimed in claim 10, or at least two modules as claimed in claim 10 coupled together [*see* Fig. 2, item 12, C 6, L 25-34].

Regarding claim 13. *Masuda et al.* teaches wherein the modules are coupled in a lateral expansion mode and/or a hierarchical mode [*see* Fig. 13, C 40-54].

Regarding claim 14. *Masuda et al.* teaches including synchronization means to facilitate data input to the neural network [*see* C 4, L 3-11 & C 18, L 56 to C 19, L 52].

Regarding claim 17. *Masuda et al.* teaches wherein an array of processing elements is implemented on the neural network device with at least one module controller [*see* C 4, L 3-11 & Fig. 7, item 200, C 11, L 39 to C 12, L 16].

6. Claims 20-21 are rejected under 35 U.S.C. 102(b) as being anticipated by *Boulet et al.* (EP 0 694 852 A1).

Regarding claim 20. *Boulet et al.* teaches a method of training a neural network [*see* page 6, L 25-59] comprising the steps of: providing a network of neurons [*see* Fig. 3(A), wherein each neuron is read an input vector applied to the input of the neural network [*see* page 6, L 25-59]; enabling each neuron to calculate its distance between the input vector and a reference vector according to a predetermined distance metric (*Examiner interprets a* metric *to be a value calculated from observed attribute values i.e., a norm that is user selectable,* wherein the neuron with the minimum distance between its reference vector and the current input becomes the active neuron [*see* page 6, L 25-L 59]; outputting the location of the active neuron [*see* page 6, L 25-59 & page 11, L 20-43]; and updating the reference vectors for all neurons located within a neighborhood around the active neuron [*see* page 6, L 25-59 & page 11, L 20-43].

Regarding claim 21. *Boulet et al.* teaches the predetermined distance metric is the Manhattan distance metric [*see* page 11, L 20-43].

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 3-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Masuda et al.* (USPN 5,165,010) in view of *Adelman et al.* (EP 0718 757 A2).

Masuda et al. has been discussed above and does not describe the limitations of claims 3-6. However, *Adelman et al.* describes the limitations of claims 3-6.

Regarding claims 3-6. *Adelman et al.* describes including data bit-size indicator means, the data bit-size indicator means enables operations on different bit-Size data values to be executed using the same instruction set, including at least one register means, the register means operates on different bit-size data in accordance with said data bit-size indicator means [*see* page 1, paragraph (57) & page 2, Summary of the Invention]. It would have been obvious at the time the invention was made to a persons having ordinary skill in the art to combine *Masuda et al.* with *Adelman et al.* because a basic operation in a DSP is a multiply/accumulate (MAC) operation. Circuits which multiply two binary numbers and add, or accumulate, the result with a third binary number are commonly used in digital signal processing [*see* page 2, L 20-24].

9. Claims 8, 9, 11, 16 & 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Masuda et al.* (USPN 5,165,010) in view of *Crosetto* (USPN 5,937,202).

Masuda et al. has been discussed above and does not describe the limitations of claims 8, 9, 11, 16 & 19. However, *Crosetto* describes the limitations of claims 8, 9, 11, 16 & 19.

Regarding claims 8, 9, 11, 16 & 19. *Crosetto* describes a programmable memory means [*see* C 3, L 32-43 & C 6, L 9-17], the memory means includes buffer memory associated with said data input means and/or said data output means, [*see* C 3, L 32-43 & C 6, L 35-48, 11. the number of processing elements in the array is a power of two [*see* C 8, L 53-58], the synchronization means includes the use of a two-line handshake mechanism [*see* C 56, L 48 to C 57, L 39 *Examiner interprets* line one to be LOAD command signal *and* line two to be FULL command signal], comprising one of the following: a full-custom very large scale integration (VLSI) device, a semi-custom VLSI device, or an application specific integrated circuit (ASIC) device [*see* Title]. It would have been obvious at the time the invention was made to a persons having ordinary skill in the art to combine *Masuda et al.* with *Crosetto* because in the recent past, front-end electronics were built with analog techniques using discrete components. Later, with the rapid advances in digital technology, Digital Signal Processors (DSPs) replaced analog circuitry up to certain speeds. However, in many applications the user still had to design a specific hardware to implement an algorithm on the front-end signal from a detector (or sensors) because the DSPs were not fast enough or feasible [*see* C 1, L 56-63].

10. Claim18 is rejected under 35 U.S.C. 103(a) as being unpatentable over *Masuda et al.* (USPN 5,165,010) in view of *Huppenthal et al.* (USPN 6,247,110). *Masuda et al.* has been discussed above and does not describe the limitations of claim 18. However, *Huppenthal et al.* describes the limitations of claim 18.

Regarding claim 18. *Huppenthal et al.* describes a field programmable gate array [*see* Abstract]. It would have been obvious at the time the invention was made to a persons having ordinary skill in the art to combine *Masuda et al.* with *Huppenthal et al.* because a multiprocessor computer architecture incorporating a number of memory algorithm processors in the memory subsystem to significantly enhance overall system processing speed [*see* C 1, L 18-21].

Claim Objection(s)

11. Claims 15, 22 & 23 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

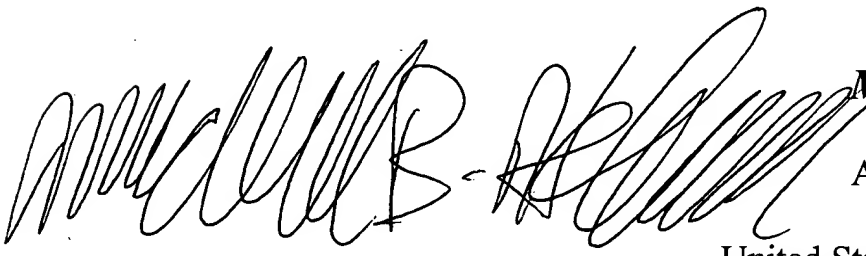
Correspondence Information

12. Any inquires concerning this communication or earlier communications from the examiner should be directed to Michael B. Holmes, who may be reached Monday through Friday, between 8:00 a.m. and 5:00 p.m. EST. or via telephone at (571) 272-3686 or facsimile transmission (571) 273-3686 or email Michael.holmesb@uspto.gov.

If you need to send an Official facsimile transmission, please send it to (703) 746-7239.

If attempts to reach the examiner are unsuccessful the Examiner's Supervisor, Anthony Knight, may be reached at (571) 272-3687.

Hand-delivered responses should be delivered to the Receptionist @ (Customer Service Window Randolph Building 401 Dulany Street Alexandria, VA 22313), located on the first floor of the south side of the Randolph Building.



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Wednesday, February 23, 2005

MBH